Claims

1. (Previously Amended) A tunneling emitter, comprising:

an electron supply;

a silicon-based dielectric layer disposed on the electron supply; and

a cathode layer disposed on the silicon-based dielectric layer;

wherein the electron supply, silicon-based dielectric layer, and cathode layer have been subjected to an annealing process to create nano-porous openings in the cathode layer.

2. (Original) The emitter of claim 1 wherein the silicon-based dielectric layer is selected from the group consisting of SiC, SiN_x, Si_3N_4, Si_xN_y, F_y-SiO_x, and C_y-SiO_x .

3. (Original) The emitter of claim 1 wherein the cathode layer is selected from the group consisting of platinum, gold, molybdenum, ruthenium, tantalum, iridium, other refractory metals and alloys thereof.

4. (Original) The emitter of claim 1 operable to provide an emitted energy with an emission current of greater than 1×10^{-2} Amps per square centimeter.

5. (Original) The emitter of claim 1 operable to provide an emitted energy with an emission current of greater than 1×10^{-1} Amps per square centimeter.

6. (Previously Amended) The emitter of claim 1 operable to provide an emission current of greater than 1×10^{0} Amps per square centimeter.

7. (Original) The emitter of claim 1 wherein the silicon-based dielectric layer has a thickness about 250 Angstroms.

8. (Original) The emitter of claim 1 wherein the silicon-based dielectric layer has a thickness less than about 500 Angstroms.

9. (Original) The emitter of claim 1 wherein the silicon-based dielectric layer has a thickness within the range of about 250 to about 5000 Angstroms.

10. (Original) An integrated circuit, comprising:

a substrate;

the emitter of claim 1 disposed on the substrate; and

circuitry for operating the emitter formed on the substrate with the emitter.

11. (Original) An electronic device, comprising:

the emitter of claim 1 capable of emitting energy; and

an anode structure capable of receiving the emitted energy and generating at least a first effect in response to receiving the emitted energy and a second effect in response to not receiving the emitted energy.

12. (Original) The electronic device of claim 11 wherein the electronic device is a mass storage device and the anode structure is a storage medium, the electronic device further comprising a reading circuit for detecting the effect generated on the anode structure.

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13. (Original) The electronic device of claim 11 wherein the electronic device is a display device and the anode structure is a display screen that creates a visible effect in response to receiving the emitted energy.

14. (Original) The electronic device of claim 13 wherein the display screen includes one or more phosphors operable for emitting photons in response to receiving the emitted energy.

15. (Previously Amended) A storage device, comprising:

at least one emitter to generate an electron beam, the emitter having a silicon-based dielectric layer having a thickness between about 250 to 5000 Angstroms, and a cathode layer disposed on the silicon-based dielectric layer, the at least one emitter subjected to an annealing process to create nano-porous openings in the cathode layer;

a lens for focusing the electron beam to create a focused beam; and

a storage medium in close proximity to the at least one emitter, the storage medium having a storage area being in one of a plurality of states to represent the information stored in that storage area;

such that:

an effect is generated when the focused beam bombards the storage area;

the magnitude of the effect depends on the state of the storage area; and

the information stored in the storage area is read by measuring the magnitude of the effect.

16. (Original) The storage device of claim 15 wherein the effect is a signal current.

17. (Previously Amended) An emitter, comprising:

an electron supply layer;

an insulator layer formed on the electron supply layer and having an opening defined within;

a silicon-based dielectric layer formed on the electron supply layer in the opening and further disposed over the insulator layer; and

a cathode layer formed on the silicon-based dielectric layer;

wherein the emitter has been subjected to an annealing process to create nano-porous openings in the cathode layer and to increase the supply of electrons tunneled from the electron supply layer to the cathode layer for energy emission.

18. (Original) The emitter of claim 17 capable of emitting photons in addition to the electron emission.

19. (Original) The emitter of claim 17 wherein the cathode layer has an emission rate greater than about 0.01 Amps per square centimeter.

20. (Original) The emitter of claim 17 wherein the silicon-based dielectric layer is selected from the group consisting of SiC, SiN_x, Si_xN_y, Si_3N_4, F_y-SiO_x, and C_y-SiO_x.

21. (Original) The emitter of claim 17 wherein the silicon-based dielectric layer has a thickness less than 500 Angstroms.

22. (Original) The emitter of claim 17 wherein the silicon-based dielectric layer has a thickness between about 250 Angstroms and about 5000 Angstroms.

23. (Original) A display device, comprising:

an integrated circuit including the emitter of claim 17, wherein the emitter creates a visible light source; and

a lens for focusing the visible light source, wherein the lens is coated with a transparent conducting surface to capture electrons emitted from the emitter.

24. (Original) A storage device, comprising:

an integrated circuit including the emitter of claim 17 wherein the emitter creates an electron beam current; and

a storage medium in close proximity to the emitter, the storage medium having a storage area being in one of a plurality of states to represent the information stored in that storage area;

such that:

an effect is generated when the electron beam current bombards the storage area;

the magnitude of the effect depends on the state of the storage area; and

the information stored in the storage area is read by measuring the magnitude of the effect.

25. (Original) An electronic device, comprising:

an integrated circuit including the emitter of claim 17; and

a focusing device for converging the emissions from the emitter.

26. (Original) A computer system, comprising:

a microprocessor;

the electronic device of claim 25 coupled to the microprocessor; and

memory coupled to the microprocessor, the microprocessor operable of executing instructions from the memory to transfer data between the memory and the electronic device.

27. (Original) The computer system of claim 26 wherein the electronic device is a storage device.

28. (Original) The computer system of claim 26 wherein the electronic device is a display device.

29. (Previously Amended) An emitter, comprising:

an electron supply surface;

an insulator layer formed on the electron supply surface and having a first opening defined within;

a silicon-based dielectric layer formed on the electron supply layer within the first, opening and further disposed on the insulator layer;

an adhesion layer disposed on the silicon-based dielectric layer, the adhesion layer defining a second opening aligned with the first opening;

a conductive layer disposed on adhesion layer and defining a third opening aligned with the first and second openings; and

a cathode layer disposed on the silicon-based dielectric layer and portions of the conductive layer, wherein the portion of the cathode layer on the silicon-based dielectric layer is an electron-emitting surface having nano-porous openings.

30. (Original) The emitter of claim 29 wherein the electron emitting surface has an emission rate of about 0.1 to about 1.0 Amps per square centimeter.

31. (Original) The emitter of claim 29, wherein the silicon-based dielectric layer is selected from the group consisting of SiC, SiN_x, Si_xN_y, Si_3N_4, F_y-SiO_x, and C_y-SiO_x.

32. (Original) The emitter of claim 29, wherein the silicon-based dielectric layer has a thickness between about 250 Angstroms to about 5000 Angstroms.

33. (Original) The emitter of claim 29, wherein the silicon-based dielectric layer has a thickness less than about 500 Angstroms.

34. (Original) The emitter of claim 29 wherein the electron supply layer is a silicon electron supply having a sheet resistance of about 100 to about 0.001 Ohms centimeter.

35. (Original) The emitter of claim 29 wherein the electron-emitting surface also emits photon energy.

36. (Previously Amended) An emitter, comprising:

an emitting surface having a first area and nano-porous openings;

a first chamber having substantially parallel sidewalls interfacing to the emitting surface; and

a second chamber interfacing to the first chamber and having sidewalls diverging to an opening having a second area larger than the first area.

37. (Original) The emitter of claim 36, further comprising a cathode layer disposed on the emitting surface, and sidewalls of the first and second chambers and wherein the emitter has been subjected to an annealing process thereby increasing the emission capability of the emitter.

38. (Original) The emitter of claim 36 wherein the first chamber is formed within an adhesion layer.

39. (Original) The emitter of claim 36 wherein the second chamber is formed within a conductive layer.

40. (Original) An integrated circuit comprising at least one emitter of claim 36.

41. (Original) A display device comprising at least one emitter of claim 36.

42. (Original) A storage device comprising at least one emitter of claim 36.

43. (Previously Amended) An integrated circuit, comprising:

a conductive surface to provide an electron supply;

at least one emitter formed on the electron supply including,

an insulator layer having at least one opening to define the location and shape of the at least one flat emitter device,

a silicon-based dielectric layer disposed within the at least one opening of the insulator layer and further disposed over the insulator layer;

a conductive layer disposed over the silicon-based dielectric layer, the conductive layer having at least one opening in alignment with the at least one opening; and

a cathode layer disposed over the silicon-based dielectric layer and partially over the conductive layer, the cathode layer having nano-porous openings.

44. (Original) The integrated circuit of claim 43 wherein the silicon-based dielectric layer has a thickness less than about 500 Angstroms.

45. (Original) The integrated circuit of claim 43 wherein the silicon-based dielectric layer has a thickness between about 250 Angstroms and about 5000 Angstroms.

46. (Original) The integrated circuit of claim 43 wherein the silicon-based dielectric layer is selected from the group consisting of SiC, SiN_x, Si_xN_y, Si_3N_4, F_y-SiO_x, and C_y-SiO_x.

47. (Original) The integrated circuit of claim 43 wherein the integrated circuit has been subjected to an annealing process.

Claims 48-63 (previously cancelled).